Guidelines:

General Guidelines:

* Mechanical Board Dimension:
* Board Thickness: <= .5mm
* Impedance controlled routing
  + 50 Ohm Single Ended
  + 100 Ohm Differential
* Trace length matched routing for high-speed signals (These signals are listed under 'FGPA->Banks')
* 01005 Capacitors/Resistors can be placed on the bottom side of the board
* **PFETs and NFETs (Q?)** can be placed on the bottom side of the board
* T1 Can be on the bottom of board
* **The current placement of the components on the board can be changed**
* The contact pads (J3) is locked in the PCB and cannot be moved
* The pads for J2 can be moved to simplify routing
* Component S1 is locked

**Sheet Specific Guidelines:**

EPM (Electro-Permanent Magnet) Sheet (Page 2)

* U4 (28V Boost Converter):
  + Place C9 as close as possible to boost converter
  + Place R13, R14 and C10 as close as possible to the IC
* All nets that carry power to the EPM should be as wide as possible, Nets include:
  + V28P0
  + EPM\_POS
  + EPMA\_NEG
  + GND

FPGA (Page 5)

* Page 5 has an example of a pin escape pattern that can be used for the ECP3 FPGA
* All Vias should be tented on the top layer underneath the FPGA
* All 01005 capacitors on page 6 should be placed underneath the FPGA.
* C60 should be placed as close as possible to U3C and U3D
* C61 should be placed as close as possible to U3B
* C72 should be placed as close as possible to U3E
* Banks (Page 7):
  + The following signals are high speed differential and should be routed as 100 Ohms differential and the signals should be matched to within 10mils.
    - TX\_P/TX\_N
    - C\_TX\_P/C\_TX\_N
    - TX\_CLK\_P/TX\_CLK\_N
    - C\_TX\_CLK\_P/C\_TX\_CLK\_N
    - RX\_P/RX\_N
    - C\_RX\_P/C\_RX\_N
    - RX\_CLK\_P/RX\_CLK\_N
    - C\_RX\_CLK\_P/RX\_CLK\_N
  + Please follow best practices when routing these high speed signals:
    - Route over a solid plane
    - where possible, the distance between differential traces (S) should be 2 X the distance between a differential trace (D):
      * As an example if a differential trace has a space between the +/- of 4 mils. The distance between a separate differential trace should be 8 mils away from the first differential trace.

Charger (Page 4)

* Place BATT1 on the right side of the board